R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Mai for the indication of allowed claims.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1-26 and 29-30 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement is respectfully traversed and should be withdrawn.

The Examiner has the initial burden to establish a reasonable basis to challenge the adequacy of the written description provided for the claimed invention (MPEP §2163.04). The conclusory statements that "The currently amended claims 1, 10 and 11 have added the limitation 'said background operations can be enabled simultaneously in each two or more of sections independently of any other section' which has no support from the originally filed specification" and "The specification only depicts a capability to refresh one-fourth, one-half, three-quarters and all of the memory array space of a DRAM" (see section 3 on pages 2-3 of the Office Action) are clearly not correct and do not adequately address the issue of why one of ordinary skill in the field of the present invention would not recognize in the Applicants' disclosure a description of the invention defined by the presently pending claims as required by MPEP §2163.04. In particular, the Office Action fails to present any evidence or

convincing line of reasoning to support the conclusion that one of ordinary skill in the field of the invention would be unable to recognize the limitation "said background operations can be enabled simultaneously in two or more of said plurality of sections independently of any other section" as being supported by the specification as originally filed (see section 3 on pages 2-3 of the Office Action).

Contrary to the position taken in the Office Action, a person of ordinary skill in the field of the invention would recognize the specification, as originally filed, as teaching that a background operation can be enabled simultaneously in two or more sections independently of any other section, as presently claimed. In particular, the specification as originally filed states:

> The present invention may be configured to control the periphery array circuitry of a number of memory array sections during a refresh operation of a memory device or apparatus. The refresh address counter (RAC) is generally configured to cycle through the address space of the memory array. The refresh address register generally controls the number of sections of the memory array that are activated during the refresh operation. For example, **to refresh one-half of the memory array of a device with four sections, the refresh block register may be configured to assert the signals REF0 and REF1 to activate the periphery array circuits of the sections 0 and 1 of the memory array.** However, other patterns of activated sections may be implemented accordingly to meet the design criteria of a particular application. By not activating the periphery array circuits of sections 2 and 3, the standby current of the device is generally reduced.
>
> The present invention may be implemented to control **other background** memory access

> **operations** and/or housekeeping operations. For example, the present invention may be configured, in one example, to control a parity checking operation of a memory array (Page 21, lines 3-21 of the specification, emphasis added).

The specification as originally filed further states:

> The present invention generally provides a method and/or an architecture for reducing the standby current of a memory device by reducing the periphery array circuitry activated during a partial array refresh. The present invention may provide, **in one example, a capability to refresh one-fourth, one-half, three-quarters, and/or all of the memory array space** of, in one example, a dynamic random access memory (DRAM). The portion of the array to be refreshed may be controlled by information (e.g., a block address) stored in a refresh address register (page 20, line 14 through page 21, line 2 of the specification, emphasis added).

A person of ordinary skill in the field of the invention would recognize, based on the above portions of the specification as originally filed, that background operations can be enabled simultaneously in (i) two sections (e.g., to refresh one-half of a four section memory array), (ii) three sections (e.g., to refresh three-quarters of a four section memory array), *etcetera*. Therefore, a person of ordinary skill in the field of the invention would recognize that the specification as originally filed describes that background operations can be enabled simultaneously in two or more of a plurality of sections, as recited in claims 1, 10 and 11.

Furthermore, possession of the claimed invention may be shown by describing the claimed invention with all of its

limitations using such descriptive means as words, structures, figures, diagrams and formulas (see MPEP §2163). A person of ordinary skill in the field of the invention would recognize, based on the drawings as originally filed (e.g., FIGS. 3 and 6), that background operations can be enabled in each of the sections 124a-d independently of any other section. In particular, a person of ordinary skill in the field of the invention would recognize that FIG. 6 as originally filed illustrates that the signals REF0-REF3 are independent of one another. Therefore, a person of ordinary skill in the field of the invention would recognize that the specification and drawings as originally filed describe that background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section, as recited in claims 1, 10 and 11. Furthermore, there is no requirement that the words used in the claims must match those used in the specification (see MPEP §§ 2163.02 and 2173.05(e)).

Because a person of ordinary skill in the field of the invention would recognize a description of the presently claimed invention in the specification and drawings as originally filed, the specification and drawings as originally filed would convey with reasonable clarity to those skilled in the field of the invention that Applicants were in possession of the presently claimed invention. Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* conclusion that there is no written description in the present specification to support claims 1-26 and 29-30. As such, the presently pending

claims 1-26 and 29-30 are fully patentable under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5-8, 10-19 and 21-26 and 29-30 under 35 U.S.C. §102(b) as being anticipated by Arimoto (U.S. Patent No. 5,798,976) is respectfully traversed and should be withdrawn.

Arimoto is directed to a semiconductor memory device with reduced current consumption in a data holding mode (Title).

In contrast to Arimoto, the presently claimed invention (claim 1) provides a method for reducing power consumption during background operations in a memory array with a plurality of sections comprising the step of controlling the background operations in each of the plurality of sections of the memory array in response to one or more control signals, where **the background operations can be enabled simultaneously in two or more of the plurality of sections independently of any other section**. Claims 10 and 11 include similar limitations.

With respect to claims 1, 10 and 11, Applicants' representative respectfully objects to the failure of the Office Action to address the specific recited claim limitation "said background operations can be enabled simultaneously in two or more sections independently of any other section" as being improper under the Patent Office's procedures as expressed in MPEP §2131.

Specifically, the rejections of claims 1, 10 and 11 do not address the specific language of the presently pending claims (see page 3, sixth and seventh line from the bottom, and page 5, lines 1-15 of the Office Action). The MPEP clearly states that TO ANTICIPATE A CLAIM, THE REFERENCE **MUST** TEACH **EVERY ELEMENT OF THE CLAIM** (MPEP §2131, capitalization original, emphasis added). Furthermore, the MPEP instructs that claims are to be examined as a whole regardless of whether a particular claim limitation is indefinite or not supported in the original specification (see MPEP §2143.03). In particular, MPEP §2143.03 states that "INDEFINITE LIMITATIONS **MUST** BE CONSIDERED" and "LIMITATIONS WHICH DO NOT FIND SUPPORT IN THE ORIGINAL SPECIFICATION **MUST** BE CONSIDERED" (MPEP §2143.03, capitalization original, emphasis added). Thus, the failure of the Office Action to address the specific limitation "said background operations can be enabled simultaneously in two or more sections independently of any other section," as recited in presently pending claims 1, 10 and 11, is not proper under the Patent Office's own procedures. As such, the rejection is not proper and should be withdrawn.

Therefore, since the rejection is not proper under the Patent Office's own procedures, it follows that the Office Action fails to meet the Office's burden of factually establishing a *prima facie* case of anticipation by factually establishing that the cited reference discloses or suggests each and every element of the presently claimed invention, arranged as in the claims (MPEP

§2131). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-9, 12-26 and 29-30 depend, directly or indirectly, from either claim 1 or claim 11 and, therefore, include the limitations of either claim 1 or claim 11. Therefore, for the reasons presented above, the Office Action fails to meet the Office's burden of factually establishing a *prima facie* case of anticipation by factually establishing that the cited reference discloses or suggests each and every element of the presently claimed invention, arranged as in the claims (MPEP §2131). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Applicants' representative respectfully requests that the Examiner clearly explain how the cited reference reads on the specific limitations of the **presently pending claims** or withdraw the rejection. Furthermore, since the Office Action fails to address the specific limitations of the presently pending claims 1, 10 and 11, the Office Action is not complete as to all matters as required by 37 C.F.R. 1.104 and, therefore, a subsequent Office Action, if issued, should not be made final.

Furthermore, despite the position taken in the Office Action, Arimoto does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. Assuming, *arguendo*, a data holding mode of Arimoto is similar to the presently claimed background operations (for which

Applicants' representative does not necessarily agree), since Arimoto states that the array control circuit 12 can "select **only one of the memory mats** when the data holding mode is designated" (column 5, lines 53-56 of Arimoto; emphasis added), it follows that Arimoto does not disclose or suggest background operations that can be **enabled simultaneously in two or more of the plurality of sections independently of any other section**, as presently claimed. Therefore, Arimoto fails to disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, the use of a decoder as taught by Arimoto (see element 12 in FIG. 5 of Arimoto) to generate the memory mat selection signals precludes more than one memory mat being enabled at a given time. Therefore, since more than one memory mat as taught by Arimoto cannot be enabled at a given time, Arimoto does not disclose or suggest background operations that can be enabled simultaneously in two or more of a plurality of sections independently of any other section, as presently claimed. Therefore, Arimoto does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-9, 12-26 and 29-30 depend, directly or indirectly, from either claim 1 or claim 11 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 27, 28 and 31 are allowed.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Registration No. 42,892
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

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